

Performance Counters and Tools

Andreas Herten, Forschungszentrum Jülich, 13 November 2017

Outline



Goals of this session

- Get to know Performance Counters
- Measure counters on POWER8
- \rightarrow Hands-on
- Additional material in appendix

Motivation Performance Counters Introduction **General Description Counters on POWER8 Measuring Counters** perf PAPI GPUs Conclusion

[...] premature optimization is the root of all evil.

- Donald Knuth

[...] premature optimization is the root of all evil. Yet we should not pass up our [optimization] opportunities [...]

– Donald Knuth

Optimization \bigcirc Measurement



Making educated decisions

Only optimize code after measuring its performance

Measure! Don't trust your gut!

Optimization () Measurement



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Measure! Don't trust your gut!

- Objectives
 - Run time
 - Cycles
 - Operations per cycle (FLOP/s)
 - Usage of architecture features (\$, (S)MT, SIMD, ...)

Optimization \bigcirc **Measurement**

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 - Usage of architecture features (\$, (S)MT, SIMD, ...)
- Correlate measurements with code
 - ightarrow hot spots/performance limiters

Optimization \bigcirc Measurement

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- Correlate measurements with code
 - \rightarrow hot spots/performance limiters
- Iterative process



Measurement



Two options for insight

Coarse Timestamps to time program / parts of program

- Only good for first glimpse
- No insight to inner workings

Detailed **Performance counters** to study usage of hardware architecture

- Instructions → CPI, IPC
 Cycles → CPI, IPC
- Floating point operations
- Stalled cycles
- Cache misses, cache hits
- Prefetches .

- Flushs
- Branches
- **CPU** migrations
- . . .

Measurement



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Detailed **Performance counters** to study usage of hardware architecture

- Instructions
 CPI, IPC
 Cycles
 CPI
- Floating point operations
- Stalled cycles
- Cache misses, cache hits
- Prefetches
- Native Derived
- Software

- Flushs
- Branches
- **CPU** migrations
- . . .



Performance Counters

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Performance Monitoring Unit



Right next to the core

- Part of processor periphery, but dedicated registers
- History
 - First occurrence: Intel Pentium, reverse-engineered 1994 (RDPMC) [1]
 - Originally for chip developers
 - Later embraced for software developers and tuners
- Operation: Certain events counted at logic level, then aggregated to registers

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Pros

- Low overhead
- Very specific requests possible; detailed information
- Information about CPU core, *nest*, cache, memory

Cons

- Processor-specific
- Hard to measure
- Limited amount of counter registers
- Compressed information content

Working with Performance Counters



Some caveats

- Mind the clock rates!
 - Modern processors have dynamic clock rates (CPUs, GPUs)
 - ightarrow Might skew results
 - Some counters might not run at nominal clock rate
- Limited counter registers
 POWER8: 6 slots for hardware counters
- Cores, Threads (OpenMP)
 - Absolutely possible
 - Complicates things slightly
 - Pinning necessary
 - \rightarrow OMP_PROC_BIND, OMP_PLACES; PAPI_thread_init()
- Nodes (MPI): Counters independent of MPI, but aggregation tool useful (Score-P, ...)



Performance Counters on POWER8

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Sources of PMU events







Sources of PMU events





Sources of PMU events



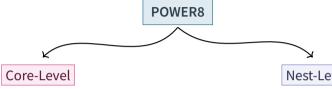
- Core / thread level
- Core pipeline analysis
 - Frontend
 - Branch prediction
 - Execution units
 - ...
- Behavior investigation
 - Stalls

. . .

Utilization



Sources of PMILevents



- Core / thread level
- Core pipeline analysis
 - Frontend
 - Branch prediction
 - Execution units
 - . . .
- **Behavior investigation**
 - Stalls

. . .

Utilization

Nest-Level

- L3 cache, interconnect fabric, memory channels
- Analysis of
 - Main memory access
 - Bandwidth



Instructions, Stalls

PM_LD_MISS_L1 Load missed L1 cache

Store: PM_ST_MISS_L1; Local L4 Hit: PM_DATA_FROM_LL4







Instructions, Stalls

 PM_LD_MISS_L1
 Load missed L1 cache Store: PM_ST_MISS_L1; Local L4 Hit: PM_DATA_FROM_LL4

 PM_INST_CMPL
 Instructions completed Also: PM_RUN_INST_CMPL

 PM_RUN_CYC
 Total cycles run Processor cycles gated by the run latch

 PM_CMPLU_STALL
 Completion stall Cycles in which a thread did not complete any groups, but there were entries

 PM_CMPLU_STALL_THRD
 Completion stall due to thread conflict After stall, thread unable to complete because other thread uses completion port

PM_GCT_NOSLOT_CYC Pipeline empty

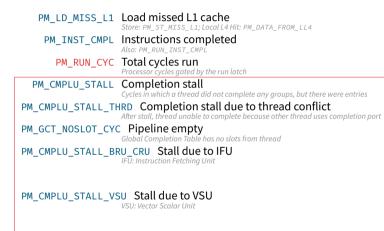
Global Completion Table has no slots from thread



PM_LD_MISS_L1	Load missed L1 cache
PM_INST_CMPL	Store: PM_ST_MISS_L1; Local L4 Hit: PM_DATA_FROM_LL4 Instructions completed Also: PM_RUN_INST_CMPL
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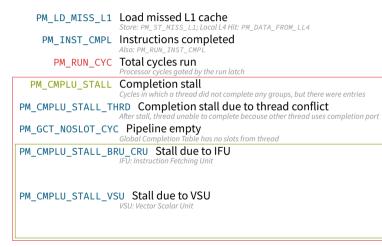


Instructions, Stalls





Instructions, Stalls



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Instructions, Stalls

PM_LD_MISS_L1	Load missed L1 cache Store: PM_ST_MISS_L1; Local L4 Hit: PM_DATA_FROM_LL4
PM_INST_CMPL	Instructions completed Also: PM RUN INST CMPL
PM_RUN_CYC	Total cycles run Processor cycles gated by the run latch
PM_CMPLU_STALL	Completion stall Cycles in which a thread did not complete any groups, but there were entries
PM_CMPLU_STALL_T	HRD Completion stall due to thread conflict After stall, thread unable to complete because other thread uses completion po
PM_GCT_NOSLOT_CY	C Pipeline empty Global Completion Table has no slots from thread
PM_CMPLU_STALL_B	RU_CRU Stall due to IFU IFU: Instruction Fetching Unit
PM_CMPLU_STALL_B	RU Stall due to BRU BRU: Branch Unit
PM_CMPLU_STALL_V	SU Stall due to VSU VSU: Vector Scalar Unit
PM_CMPLU_STALL_S	CALAR_LONG Stall due to long scalar instruction Floating point divide or square root instructions

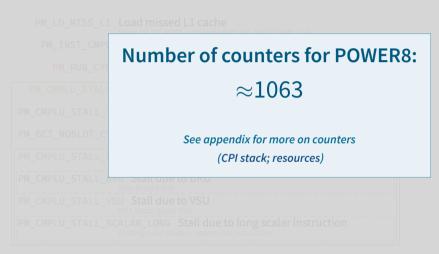


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PM_CMPLU_STALL_VS	SU Stall due to VSU VSU: Vector Scalar Unit			
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Measuring Counters

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perf Linux' tool (also called perf_events)
PAPI C/C++ API
Score-P Measurement environment (appendix)
Likwid Set of command line utilities for detailed analysis
perf_event_open() Linux system call from linux/perf_event.h
... Many more solutions, usually relying on perf

perf

Linux' own performance tool

- Part of Linux kernel since 2009 (v. 2.6.31)
- Example usage: perf stat ./app

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\$ perf stat ./poisson2d
Performance counter stats for './poisson2d':

65703.208586	task-clock (msec)	#	1.000 CPUs utilized	
355	context-switches		0.005 K/sec	
	cpu-migrations		0.000 K/sec	
10,847	page-faults		0.165 K/sec	
228,425,964,399	cycles		3.477 GHz	(66.67%)
299,409,593	stalled-cycles-frontend		0.13% frontend cycles idle	(50.01%)
147,289,312,280	stalled-cycles-backend		64.48% backend cycles idle	(50.01%)
323,403,983,324	instructions		1.42 insn per cycle	
			0.46 stalled cycles per insn	(66.68%)
12,665,027,391	branches		192.761 M/sec	(50.00%)
4,256,513	branch-misses		0.03% of all branches	(50.00%)

65.715156815 seconds time elapsed



perf



Linux' own performance tool

- Part of Linux kernel since 2009 (v. 2.6.31)
- Usage: perf stat ./app
- Raw counter example: perf stat -e r600f4 ./app

\$ perf stat -e r600f4 ./poisson2d Performance counter stats for './poisson2d': 228,457,525,677 r600f4 65.761947405 seconds time elapsed

perf



Linux' own performance tool

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- Raw counter example: perf stat -e r600f4 ./app
- More in appendix



PAPI



Measure where it hurts...

- Performance Application Programming Interface
- API for C/C++, Fortran

PAPI



Measure where it hurts...

- Performance Application Programming Interface
- API for C/C++, Fortran
- Goal: Create common (and easy) interface to performance counters
- Two API layers (Examples in appendix!)
 - High-Level API: Most-commonly needed information capsuled by convenient functions
 - Low-Level API: Access all the counters!



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- Command line utilities

papi_avail List aliased, common counters

Use papi_avail -e EVENT to get description and options for EVENT papi_native_avail List all possible counters, with details

Extendable by Component PAPI (GPU!)



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- Extendable by Component PAPI (GPU!)
- Comparison to perf: Instrument specific parts of code, with different counters

papi_avail

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\$ papi_avail

Available PAPI preset and user defined events plus hardware information.

PAPI Version	5.5.0.0
Vendor string and code	IBM (3)
Model string and code	8335-GCA
CPU Revision	2.000000
CPU Max Megahertz	3491
CPU Min Megahertz	2061
Hdw Threads per core	8
Cores per Socket	10
Sockets	2
NUMA Nodes	1
CPUs per Node	160
Total CPUs	160
Running in a VM	no
Number Hardware Counters	6



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papi_avail

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Max Multiplex Counters : 192

PAPI Preset Events

Name	Code	Avail	Deriv	Description (Note)
PAPI_L1_DCM	0x80000000	Yes	Yes	Level 1 data cache misses
PAPI_L1_ICM	0x80000001	Yes	No	Level 1 instruction cache misses
PAPI_L2_DCM	0x80000002	Yes	No	Level 2 data cache misses
PAPI_L2_ICM	0x80000003	No	No	Level 2 instruction cache misses
PAPI_L3_DCM	0x80000004	No	No	Level 3 data cache misses
PAPI_L3_ICM	0x80000005	Yes	No	Level 3 instruction cache misses
PAPI_L1_TCM	0x80000006	No	No	Level 1 cache misses
PAPI_L2_TCM	0x80000007	No	No	Level 2 cache misses
PAPI_L3_TCM	0x80000008	No	No	Level 3 cache misses
PAPI_CA_SNP	0x80000009	No	No	Requests for a snoop

papi_avail



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\$ papi_avail -e PM_DATA_FROM_L3MISS Available PAPI preset and user defined events plus hardware information.

Event name: Event Code: Number of Register Values: Description:	PM_DATA_FROM_L3MISS 0x40000011 0 Demand LD - L3 Miss (not L2 hit and not L3 hit).
Unit Masks:	
Mask Info:	:u=0 monitor at user level
Mask Info:	:k=0 monitor at kernel level
Mask Info:	<pre> :h=0 monitor at hypervisor level </pre>
Mask Info:	:period=0 sampling period
Mask Info:	:freq=0 sampling frequency (Hz)
Mask Info:	:excl=0 exclusive access
Mask Info:	<pre> :mg=0 monitor guest execution </pre>



Notes on usage; Tipps

Important functions in High Level API

PAPI_num_counters() # available counter registers
PAPI_flops() Get real time, processor time, # floating point operations, and MFLOPs/s
PAPI_ipc() # instructions and IPC (+rtime/ptime)
PAPI_epc() # counts of arbitrary event (+rtime/ptime)

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Important functions in Low Level API

PAPI_add_event() Add aliased event to event set
PAPI_add_named_event() Add any event to event set
PAPI_thread_init() Initialize thread support in PAPI

Documentation online and in man pages (man papi_add_event)



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- \rightarrow http://icl.cs.utk.edu/papi/



- Counters built right in
- Grouped into domains by topic
- NVIDIA differentiates between (more examples in appendix)

Event Countable activity or occurrence on GPU device Examples: shared_store, generic_load, shared_atom Metric Characteristic calculated from one or more events Examples: executed_ipc, flop_count_dp_fma, achieved_occupancy

- Usually: access via nvprof / Visual Profiler; but exposed via CUPTI for 3rd party
- ightarrow Afternoon session / appendix





What we've learned

- Large set of performance counters on POWER8 processors
- Right next to (*inside*) core(s)
- Provide detailed insight for performance analysis on many levels
- Different measurement strategies and tools
 - perf
 - PAPI
 - Score-P
- Also on GPU

Thank you for your attention!

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Large set of performance counters on POWER8 processors

- Right next to (inside) core(s)
- Provide detailed insight for performance analysis on many levels

bit.ly/sc17-eval

- Different measurement strategies and tools
 - perf

Conclusions What we've learned

- PAPI
- Score-P
- Also on GPU





Appendix Knuth on Optimization POWER8 Performance Counters perf PAPI Supplementary Score-P GPU Counters Glossary References

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Appendix Knuth on Optimization

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The full quote, finally

There is no doubt that the grail of efficiency leads to abuse. Programmers waste enormous amounts of time thinking about, or worrying about, the speed of noncritical parts of their programs, and these attempts at efficiency actually have a strong negative impact when debugging and maintenance are considered. We should forget about small efficiencies, say about 97 % of the time: pre mature optimization is the root of all evil.

Yet we should not pass up our opportunities in that critical 3 %. A good programmer will not be lulled into complacency by such reasoning, he will be wise to look carefully at the critical code; but only after that code has been identified

- Donald Knuth in "Structured Programming with Go to Statements" [2]



Appendix POWER8 Performance Counters

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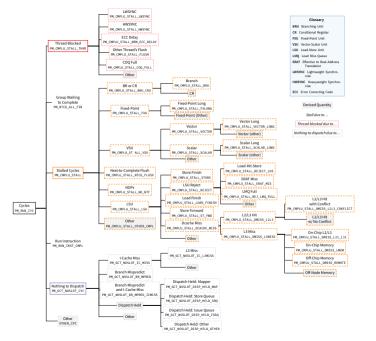
POWER8 Performance Counters



- Further information on counters at IBM website
 - JSON overview of OpenPOWER PMU events on Github
 - CPI events and metrics for POWER8
 - Events and groups supported on POWER8 architecture
 - Derived metrics defined for POWER8 architecture
 - Table 11-18 and Table D-1 of POWER8 Processor User's Manual for the Single-Chip Module
 - OProfile: ppc64 POWER8 events
- List available counters on system
 - With PAPI: papi_native_avail
 - With showevtinfo from libpfm's /examples/ directory
 - ./showevtinfo | 🔪

```
grep -e "Name" -e "Desc" | sed "s/^.\+: //g" | paste -d'\t' - -
```

- See next slide for CPI stack visualization
- Most important counters for OpenMP: DMISS_PM_CMPLU_STALL_DMISS_L3MISS, PM_CMPLU_STALL_DMISS_REMOTE, PM_CMPLU_STALL_DMISS_DISTANT





$\underset{_{\text{perf}}}{\text{Appendix}}$

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perf Sub-commands



Sub-commands for perf

perf list List available counters
perf stat Run program; report performance data
perf record Run program; sample and save performance data
perf report Analyzed saved performance data (appendix)
 perf top Like top, live-view of counters



perf *Tipps, Tricks*

Option -- repeat for statistical measurements

1.239 seconds time elapsed (+- 0.16%)

- Restrict counters to certain user-level modes by -e counter:m, with m = u (user), = k (kernel), = h (hypervisor)
- perf modes: Per-thread (default), per-process (-p PID), per-CPU (-a)
- Other options
 - -d More details
 - -d -d More more details
- More info
 - web.eece.maine.edu/~vweaver/projects/perf_events/
 - Brendan Gregg's examples on perf usage
- \rightarrow https://perf.wiki.kernel.org/

- -B Add thousands' delimiters
- -x Print machine-readable output

Deeper Analysis with perf

perf record

Usage: perf record ./app

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\$ perf record ./poisson2d [perf record: Woken up 41 times to write data] Inf_contrack_ipv4] with build id ada66fe00acc82eac85be0969a935e3167b09c88 not found, continuing without symbols Inf_contrack] with build id 2911e97a3bde3302788e8388d1e3c19408ad86cf not found, continuing without symbols [ebtables] with build id b0aa834b86d596edeb5a72d1ebf3936a98b17bcf not found, continuing without symbols [ip_tables] with build id 23fe04e7292b66a2cc104e8c5b026b4b3a911cac not found, continuing without symbols [bridge] with build id b7a0fcdbca63084c22e04fcf32e0584d04193954 not found, continuing without symbols [bridge] with build id b7a0fcdbca63084c22e04fcf32e0584d04193954 not found, continuing without symbols [perf record: Captured and wrote 10.076 MB perf.data (263882 samples)]

\$ ll perf.data
-rw----- 1 aherten zam 10570296 Aug 26 19:24 perf.data



Deeper Analysis with perf

perf report: Overview



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Solk of event 'cycles:pp'; truet count (approx.): 22805603717, Thread: poisson2 Solk of event 'cycles:pp'; truet count (approx.): 22805603717, Thread: poisson2 Solk of event 'cycles:pp'; truet count (approx.): 22805603717, Thread: poisson2 Solk of poisson2 [.] main A.78< poisson2 libe:2.17.50 [.]marf A.21% poisson2 libe:2.17.50 [.]marf A.21% poisson2 libe:2.17.50 [.]marf A.21% poisson2 libe:2.17.50 [.]marf A.01% poisson2 libe:2.17.50 [.]					
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Deeper Analysis with perf



perf report:Zoomtomain()

ain /oni	fs/homeh/za	n/aherten/NVAL/OtherProgramming/OpenPOWER-SC17/PAPI-Test/poisson2d		
0.00		r9,100(r31)	1	
		r9,r18,r9	i	
		r9,r9	i	
		r10,140(r31)	i	
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		r9, r9	1	
		r10,140(r31)	1	
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0.00				
	rldicr	r9,r9,3,60	I	
0.00		r10,168(r31)	I	
		r9,r10,r9	1	
22.54		f0,8(r9)	I	
0.01	fsub	f0,f12,f0	I	
0.00	fabs	f0,f0	I	
0.00		f2,f0	I	
		f1,128(r31)	I	
	bl ld	10000780 <00000017.plt_call.fmax@QGLIBC_2.17> r2,24(r1)		



Appendix PAPI Supplementary

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PAPI: High Level API

Usage: Source Code

// Setup
float realTime, procTime, mflops, ipc;
long long flpins, ins;

// Initial call PAPI_flops(&realTime, &procTime, &flpins, &mflops); PAPI_ipc(&realTime, &procTime, &ins, &ipc);

// Compute
mult(m, n, p, A, B, C);

// Finalize call

PAPI_flops(&realTime, &procTime, &flpins, &mflops); PAPI_ipc(&realTime, &procTime, &ins, &ipc);



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PAPI: Low Level API

Usage: Source Code

int EventSet = PAPI_NULL; long long values[2];

// PAPI: Setup

```
PAPI library init(PAPI VER CURRENT):
PAPI create eventset(&EventSet);
// PAPI: Test availability of counters
PAPI_query_named_event("PM_CMPLU_STALL_VSU");
PAPI guery named event("PM CMPLU STALL SCALAR"):
// PAPI: Add counters
PAPI add named event(EventSet, "PM CMPLU STALL VSU");
PAPI add named event(EventSet. "PM CMPLU STALL SCALAR"):
// PAPI: Start collection
PAPI_start(EventSet);
// Compute
do_something();
// PAPI: End collection
PAPI_CALL( PAPI_stop(EventSet, values) , PAPI_OK );
```



PAPI: Low Level API

Usage: Source Code

int EventSet = PAPI_NULL; long long values[2];

// PAPI: Setup PAPI library init(PAPI VER CURRENT): PAPI create eventset(&EventSet); // PAPI: Test availability of counters PAPI_query_named_event("PM_CMPLU_STALL_VSU"); PAPI guery named event("PM CMPLU STALL SCALAR"): // PAPI: Add counters PAPI add named event(EventSet, "PM CMPLU STALL VSU"); Pre-processor macro PAPI add named event(EventSet. "PM CMPLU STALL SCALAR" for checking results! // PAPI: Start collection See next slides! PAPI_start(EventSet); // Compute do_something(); // PAPI; End collection PAPI_CALL(PAPI_stop(EventSet, values) , PAPI_OK);



PAPI Error Macro: C++



For easier status code checking

```
#include "papi.h"
#define PAPI_CALL( call, success )
    int err = call:
    if ( success != err)
    std::cerr << "PAPI error for " << #call << " in L" << __LINE__ << " of " <<
→ __FILE__ << ": " << PAPI_strerror(err) << std::endl; \
// Second argument is code for GOOD,
// e.g. PAPI_OK or PAPI_VER_CURRENT or ...
// ...
// Call like:
PAPI_CALL( PAPI_start(EventSet), PAPI_OK );
```

PAPI Error Macro: C



For easier status code checking

```
#include "papi.h"
#define PAPI_CALL( call, success )
    int err = call:
    if ( success != err)
    fprintf(stderr, "PAPI error for %s in L%d of %s: %s\n", #call, __LINE__,
→ ___FILE__, PAPI_strerror(err)); \
// Second argument is code for GOOD,
// e.g. PAPI_OK or PAPI_VER_CURRENT or ...
// ...
// Call like:
PAPI_CALL( PAPI_start(EventSet), PAPI_OK );
```





- Helper library for setting up counters interfacing with perf kernel environment
- Used by PAPI to resolve counters
- Handy as translation: Named counters \rightarrow raw counters
- Use command line utility perf_examples/evt2raw to get raw counter for perf

\$./evt2raw PM_CMPLU_STALL_VSU r2d012

 \rightarrow http://perfmon2.sourceforge.net/docs_v4.html



Appendix _{Score-P}

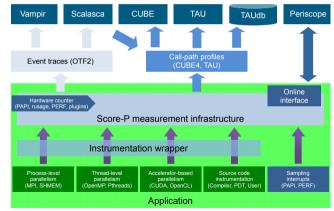
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Introduction



- Measurement infrastructure for profiling, event tracing, online analysis
- Output format input for many analysis tools (Cube, Vampir, Periscope, Scalasca, Tau)



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Howto



Prefix compiler executable by scorep



- ightarrow Adds instrumentation calls to binary
- Profiling output is stored to file after run of binary
- Steer with environment variables at run time

•••

\$ export SCOREP_METRIC_PAPI=PAPI_FP_OPS,PM_CMPLU_STALL_VSU
\$./app

- \Rightarrow Use different PAPI counters per run!
- Quick visualization with Cube; scoring with scorep-score



Principle analysis with scorep-score

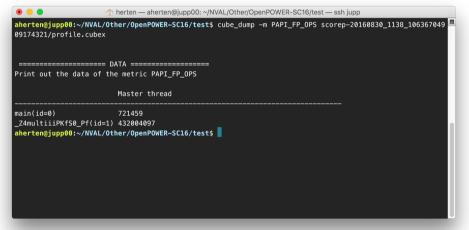
Usage: scorep-score -r FILE

60348578	307/profil		n / openro	WER-3	CIO/LESL\$	scorep-score	-r -c 2 scorep-20160826_2106_1032520
Fstimate	ed aggrega	te size d	of event	trace		140	9 bytes
						(max_buf): 149	
	ed memory						97kB
							ntermediate flushes
or real	ice requir	ements us	ing USR	regio	ns filter	5.)	
flt	type max	buf[B] vi	lsits tim	e[s]	time[%] t:	ime/visit[us]	region
	ALL	148		1.92	100.0		
	USR	148	2	1.92	100.0	961066.48	USR
	USR	74	1	1.89	98.4	1891933.34	_Z4multiiiPKfS0_Pf
		74	1	0.03	1.6	30199.62	main
	USR						



Performance counter analysis with cube_dump

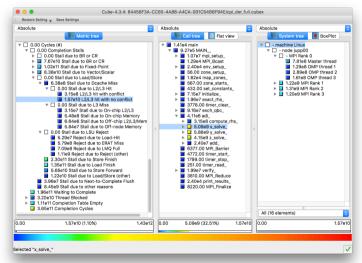
Usage: cube-dump -m METRIC FILE



Score-P



Analysis with Cube





Appendix GPU Counters

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GPU Example Events & Metrics



- gld_inst_8bit Total number of 8-bit global load instructions that are executed by all the threads across all thread blocks.
- threads_launched Number of threads launched on a multiprocessor.
 - inst_executed Number of instructions executed, do not include replays.
 - shared_store Number of executed store instructions where state space is specified as shared, increments per warp on a multiprocessor.
 - executed_ipc Instructions executed per cycle
- achieved_occupancy Ratio of the average active warps per active cycle to the maximum number of warps supported on a multiprocessor
- l1_cache_local_hit_rate Hit rate in L1 cache for local loads and stores
 - gld_efficiency Ratio of requested global memory load throughput to required global memory load throughput.
- stall_pipe_busy Percentage of stalls occurring because a compute operation cannot be performed because the compute pipeline is busy

Measuring GPU counters

Tools



CUPTI C/C++-API through cupti.h

- Activity API: Trace CPU/GPU activity
- Callback API: Hooks for own functions
- Event / Metric API: Read counters and metrics
- $ightarrow \,$ Targets developers of profiling tools
- PAPI All PAPI instrumentation through PAPI-C, e.g. cuda:::device:0:threads_launched
- Score-P Mature CUDA support
 - Prefix nvcc compilation with scorep
 - Set environment variable SCOREP_CUDA_ENABLE=yes
 - Run, analyze

nvprof, Visual Profiler NVIDIA's solutions

nvprof *GPU command-line measurements*



Usage: nvprof --events AB --metrics C,D ./app

🖲 😑 👘 🏫 herten		CUDA-7.5_Samples/bin/	x86_64/linux/release -	linux/release	— ssh juhydra	
at*, int, int)" (0 of 3)= ==18158== Replaying kerne ixMulCUDA <int=32>(float*, at*, int, int)" (0 of 3)= Performance= 1.69 GFlop/s</int=32>	<pre>float*, float*, int, int)" (0 of 3)== =B155e= Replaying kernel "void matri: 1 "void matri:B2C+float*, float*, float*, int, int)" (0 of 3)== =B155e= Replaying kernel "void matri: 7 ime= 77.513 mece, 5ize= 131072000 (for correctness: Result = PASS</pre>	xMulCUDA <int=32>(1 float*, float*, i =18158== Replaying xMulCUDA<int=32>(1</int=32></int=32>	float*, float*, f int, int)" (0 of 3 g kernel "void ma float*, float*, f	loat*, int, 3)==18158== trixMulCUDA< loat*, int,	int)" (done) Replaying ke int=32>(floa	rnel "void mat
NOTE: The CUDA Samples are not meant for performance measurements. Results may vary when GPU Boost is enabled. ==18158== Profiling result: ==18158== vent result:						
Invocations	Event Name 🕴	Min Max	Avg			
Device "Tesla K40m (0)"						
Kernel: void matrixMulCUDA <int=32>(float*, float*, float*, int, int)</int=32>						
301	threads_launched 2044	800 204800	204800			
==18158== Metric result:						
Invocations	Metric Name	Met	tric Description	Min	Max	Avg
Device "Tesla K40m (0)"						
Kernel: void matrixMulCUDA≺int=32>(float*, float*, float*, int, int)						
301	flop_count_sp Floating	g Point Operations	s(Single Precisi	131072000	131072000	131072000
301	ipc		Executed IPC	1.472345	1.486837	1.480249
301	achieved_occupancy	Act	nieved Occupancy	0.960357	0.989658	0.975385
<pre># aherten @ JUHYDRA in ~/cudaSamples/NVIDIA_CUDA-7.5_Samples/bin/x86_64/linux/release [21:47:45] \$ nvprofevents threads_launchedmetrics flop_count_sp.jpc,achieved_occupancy ./matrixHul</pre>						



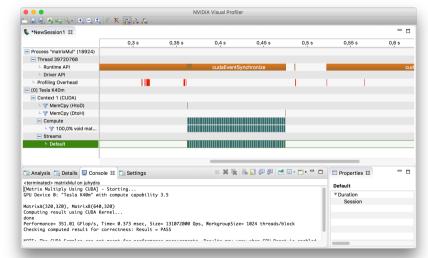
Useful parameters to nvprof

- --query-metrics List all metrics
 - --query-events List all events
- --kernels name Limit scope to kernel
- --print-gpu-trace Print timeline of invocations
- --aggregate-mode off No aggregation over all multiprocessors (average)
 - --csv Output a CSV
 - --export-profile Store profiling information, e.g. for Visual Profiler

Visual Profiler



An annotated time line view

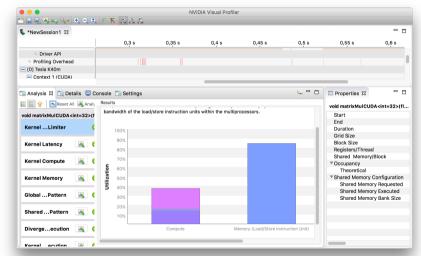


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Visual Profiler



Analysis experiments





Appendix Glossary & References

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Glossary I



CPI Cycles per Instructions; a metric to determine efficiency of an architecture or program. 9, 10

IPC Instructions per Cycle; a metric to determine efficiency of an architecture or program. 9, 10

MPI The Message Passing Interface, a API definition for multi-node computing. 14

NVIDIA US technology company creating GPUs. 46, 75, 76

OpenMP Directive-based programming, primarily for multi-threaded machines. 14

Glossary II



PAPI The Performance API, a C/C++ API for querying performance counters. 2, 31, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 47, 48

- perf Part of the Linux kernel which facilitates access to performance counters; comes with command line utilities. 2, 31, 32, 33, 34, 35, 36, 37, 38, 47, 48
- POWER8 CPU architecture from IBM, available also under the OpenPOWER Foundation. 2, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 47, 48, 49, 52, 53
- Score-P Collection of tools for instrumenting and subsequently scoring applications to gain insight into the program's performance. 31, 47, 48

CPU Central Processing Unit. 9, 10, 12, 13, 14, 82





GPU Graphics Processing Unit. 14, 35, 36, 37, 38, 46, 47, 48, 82

PMU Performance Measuring Unit. 16, 17, 18, 19

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The End

Thanks for reading until here!

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